I claim:

1. A process for producing a predetermined area with two adjacent regions in an integrated semiconductor such that a first region of the two adjacent regions has a target concentration of a dopant that is lower than a target concentration of the dopant in a second region of the two adjacent regions, the process which comprises:

applying a polysilicon layer to a semiconductor blank;

forming a window in the polysilicon layer such that the window defines a predetermined area of the semiconductor blank;

doping the predetermined area of the semiconductor blank with the dopant until a concentration of the dopant is at least as high as the target concentration of the second region;

forming a spacer in a self-adjusting manner with respect to an edge of the window such that the spacer defines the second region; and

diffusing the dopant outward from the first region until the concentration of the dopant corresponds to the target concentration of the first region.

2. The process according to claim 1, which comprises performing the doping by implantation.

3. The process according to claim 2, which comprises: after the doping step and before forming the spacer, tempering the predetermined area.

4. The process according to claim 3, which comprises performing outward diffusion by tempering until a concentration of the dopant corresponds to the target concentration of the second region.

5. The process according to claim 1, wherein the dopant is selected from the group consisting of boron, aluminum, gallium, indium, phosphorus, arsenic, and antimony.

6. The process according to claim 1, wherein the step of diffusing the dopant outward is performed by tempering.

7. The process according to claim 1, which comprises providing the predetermined area as a base area of a transistor.

8. The process according to claim 7, which comprises providing the first region as a base region of an active transistor.

9. The process according to claim 8, which comprises providing the second region as a link region between a base region and a polysilicon track.

10. The process according to claim 7, which comprises providing the second region as a link region between a base region and a polysilicon track.

11. The process according to claim 1, which comprises: after the doping step and before forming the spacer, tempering the predetermined area.

12. The process according to claim 1, which comprises:

producing an integrated transistor, in which the second region forms a base area underneath a spacer surrounding an emitter; and

the first region forms a base area under the emitter.

13. An integrated transistor, comprising:

an emitter, a collector, and a base;

a polysilicon layer provided as a base contact, said polysilicon layer having an edge; and

a spacer formed on said edge of said polysilicon layer and surrounding said emitter;

said base having a base area under said spacer and a base area under said emitter;

said base area under said spacer being more highly doped than said base area under said emitter;

said base area under said spacer being formed in a self-adjusting manner in relation to said spacer.